Is That an FPGA in Your Embedded System or an Embedded System in My FPGA?

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Agenda

- FPGAs in RT Embedded Systems Today
- A Platform Approach to RTEC
- Future Directions in RTEC
Typical RTEC Applications with FPGAs

- **Aerospace and Defense**
  - Guidance Systems
  - Surveillance and Secure Communications

- **Communications**
  - Baseband Processing

- **Industrial Command & Control**
  - Machine Vision
  - Motor Control

- **Automotive**
  - Driver Assistance
  - Safety
The Supporting Role of FPGAs in RTEC Today

- Delivering Mission Critical Performance
  - Parallel Processing
  - High Bandwidth
  - Low Latency

- High-Speed, Industry Standard Connectivity

- System Integration

- Flexibility
  - Adapts to Varying Market Requirements
Case 1: Automotive Image Processing

Input Image
Pre-Processed Image
Identified Element
Driver Warning

FPGA
Pre-Processing (Pixel Level)
Image Capture, Noise Filtering, Contrast Enhancement, etc.

Discrete DSP
Analytics Processing (Element Level)
Object Detection / Classification, Pattern Recognition, etc.

GPP
Application Processing, System Control
Situational Assessment & Warning Decision, Sensor Control, etc.
Case 2: Traditional 3G Wireless Base Station

- Implement All PHY Functions in FPGA
- Remove DSP
- 2-processor Solution Reduces Cost and Improves Power Efficiency

- Network Processor
  - RLC
  - MAC Scheduling
  - Board Control

- DSP
  - PHY Processing

- FPGA Co-Processor
  - Turbo Decoder
  - DFT, FFT, RACH

- Heavy Lifting Moved to FPGA Co-processor
- Other Functions Remain on the DSP
- 3-processor Solution is Not Cost or Power Efficient
- Data Interface Between DSP and FPGA Becomes an Issue with LTE
Case 3: Video Surveillance for UAV System

- Real-time Image Processing
  - Noise Filtering and Segmentation
  - Motion Detection

- All Processing Performed by a Single FPGA

- DSP Image Processing
- GPP System Management
- Compression Co-processor
- Memory Controller
- Data Transmission
- Secret Sauce
FPGA Implementation Challenges for RTEC Teams

- **Architect**
  - Picking the Right Architecture, Processor
  - HW/SW Partitioning

- **HW Designer**
  - Hand-crafting RTL for Parallel DSP Acceleration
  - IP Availability and Integration from Multiple Sources
  - Cross-domain Development/Debug

- **Software Developer**
  - Waiting for HW Before SW Development
  - Code Optimization
  - HW/SW Co-debug
What’s Needed in Next-Generation RTEC Systems

- Lower System Power
- Higher Performance
- Higher Integration
- Reduced System Cost
- Better Scalability

Better Products

- Plug & Play IP Inter-operability
- Design Re-use
- Ease of Programming
- Extensive Ecosystem

Better Productivity
A Platform Approach to RT Embedded Computing
The Xilinx Vision
Targeted Design Platforms

- Enhanced Ecosystem(s)
- Interchangeable “Socketable IP”
- Unified Open Standard Adoption
- Domain-specific Methodologies
- Targeted Reference Designs

Robust ecosystem delivering a system of interdependent capabilities to solve existing and new challenges
Anatomy of an Embedded Processing Kit

- The Right Processor Architecture
- The Right Interconnect
- Robust Mix of Peripherals and IP
- Familiar Development Environment
  - SOC Development
  - Code Development
  - Debug

- Scalable Base Board with FMC
- Domain Optimized Design Environment
- Targeted Reference Designs
- Documentation, Source Code, and IP Cores
Example: RTC in Industrial Control Systems
Realtime Networking and Machine Vision on the Factory Floor
Example of Industrial Control Design Kit

Enabling RTEC Designers to Innovate Faster…

Platform Elements

**Market-specific**
- Real-time Ethernet Reference Designs
- Embedded Application Stack
- Real-time Ethernet IP Slave

**Domain-specific**
- Soft Processor IP
- Software Development Tools
- DSP Development Tools
- Industrial Network Daughter Card
- Ethernet 802.3 Support

**Base Platform**
- FPGA Device and Base Board
- Hardware Design Tools
- Reference Designs and IP
Example of Single-Chip Crypto (SCC) Design Kit

Platform Elements

Market-Specific
- Isolation Verification Tool
- Secure Design App Notes
- SCC Design Guide
- ISO Flow User Guide
- Partial Reconfiguration Guide
- SCC Verification Services

Domain-Specific
- Embedded Processing Kit
- DSP IP
- Connectivity IP
- Design Planning Tools

Base Platform
- FPGA Device and Base-board
- Hardware Design Tools
Future Directions in RTEC
Partnering with Industry Leaders
ARM and Xilinx Alliance – Oct 2009

- Industry’s Most Popular Embedded Processor & Roadmap
- Optimized Interconnect Standard For FPGAs
  - Next-generation AMBA
- ARM Connected Community and Xilinx Partners
- Robust Ecosystem of Tools, IP and Programmers
- Two Targets:
  - Embedded Processing Domain
  - Programmable Logic Innovation

Microprocessor Forum “Many to Few”
Next-Generation AMBA Innovation

- **Replaces Many Different Interfaces on FPGAs**
  - Delivers Ease of Use and Enables Compatibility
  - Single Industry-standard Interface
    - Only Need to Know One Family of Interfaces, Regardless of Whether They’re Embedded, DSP or Logic Users

- **Choice and Time to Market**
  - Greater Catalog of IP Leads to Faster Time to Market

- **Options to Optimize**
  - Low-latency, Streaming, Light-weight
  - Improved Embedded Performance over Current Interfaces

- **Enables Multiple Use Models:**

  - **Processor Internal**
    - Processor
    - Partner IP
    - Xilinx IP
    - FPGA

  - **Processor External**
    - Xilinx IP
    - Partner IP
    - FPGA

  - **“Processor-less”**
    - Xilinx IP
    - Partner IP
    - FPGA
What the Xilinx/ARM Alliance Will Deliver

- Targeted Design Platforms Based on Leading 32-bit Processor Roadmap
- AMBA Next-generation Interconnect Optimized for FPGA Fabric
  - Improves Fabric Optimization and Performance
  - Enables “Socketable IP”
- ARM Connected Community ↔ Partner Ecosystem
  - Broad IP Catalog
  - Popular RTOSs, Drivers, IDEs

✓ Better RTEC Products
✓ Better Productivity
More Key Developments for RTEC

- Heterogeneous Multiprocessing
- System Power Optimization
- ESL
  - Electronic System Virtualization
  - High-level DSP Synthesis
**BDTI Benchmarks of ESL Synthesis for DSP**

**HLST QoR Is 30x Better Than DSP’s for Our Video Application**

Preliminary results for the BDTI Optical Flow Workload, Operating Point 2: maximum frame rate achievable at 720p resolution

![Graph](image1.png)

**HLST QoR Is Equivalent to Hand-Written RTL for Our Wireless Application**

Preliminary results for the BDTI DQPSK Receiver Workload, 18.75 Msamples second input data with a 75 MHz clock

![Graph](image2.png)

These results are consistent with those reported by HLST users interviewed by BDTI.

**Key findings:**

- Similar total effort required for DSP and HLST+FPGA implementations
- Different skills required...
The Expanding Role for FPGAs in RTEC

- A Platform Approach will Accelerate Development
- AMBA Interconnect on FPGAs will Enhance the RTEC Landscape and Significantly Grow the Ecosystem
- Future Innovations in ESL and Multicore will Further Increase Productivity
Thank you
Easily Extend Functionality

• Use Base TDP Networking Platform
• Add Imaging Analytics Functionality with Networking
• Bitstream and Bridging Cameralink to IP -
• With FMC for Machine Vision Extension
Other Segment TDPs in Development
LTE eNodeB Targeted Design Platform

Scalable to the Design Platform Requirements